

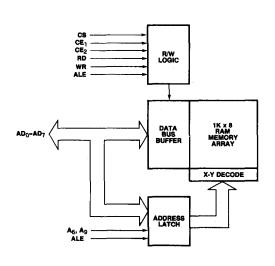
8185/8185-2 1024 x 8-BIT STATIC RAM FOR MCS-85°

- Multiplexed Address and Data Bus
- Directly Compatible with 8085A and IAPX 88 Microprocessors
- Low Operating Power Dissipation
- **Low Standby Power Dissipation**
- Single +5V Supply
- High Density 18-Pin Package

The Intel® 8185 is an 8192-bit static random access memory (RAM) organized as 1024 words by 8-bits using N-channel Silicon-Gate MOS technology. The multiplexed address and data bus allows the 8185 to interface directly to the 8085A and IAPX 88 microprocessors to provide a maximum level of system integration.

The low standby power dissipation minimizes system power requirements when the 8185 is disabled.

The 8185-2 is a high-speed selected version of the 8185 that is compatible with the 5 MHz 8085A-2 and the full speed 5 MHz IAPX 88.







AD ₀ -AD ₇	ADDRESS/DATA LINES
Ag, Ag	ADDRESS LINES
CS	CHIP SELECT
CE ₁	CHIP ENABLE (IO/M)
CE ₂	CHIP ENABLE
ALE	ADDRESS LATCH ENABLE
WR	WRITE ENABLE

Figure 2. Pin Configuration



FUNCTIONAL DESCRIPTION

The 8185 has been designed to provide for direct interface to the multiplexed bus structure and bus timing of the 8085A microprocessor.

At the beginning of an 8185 memory access cycle, the 8-bit address on AD₀₋₇, A₈ and A₉, and the status of \overline{CE}_1 and CE₂ are all latched internally in the 8185 by the falling edge of ALE. If the latched status of both \overline{CE}_1 and CE₂ are active, the 8185 powers itself up, but no action occurs until the \overline{CS} line goes low and the appropriate \overline{RD} or \overline{WR} control signal input is activated.

The $\overline{\text{CS}}$ input is not latched by the 8185 in order to allow the maximum amount of time for address decoding in selecting the 8185 chip. Maximum power consumption savings will occur, however, only when $\overline{\text{CE}}_1$ and CE_2 are activated selectively to power down the 8185 when it is not in use. A possible connection would be to wire the 8085A's $\overline{\text{IO}/M}$ line to the 8185's $\overline{\text{CE}}_1$ input, thereby keeping the 8185 powered down during I/O and interrupt cycles.

Table 1.
Truth Table tor
Power Down and Function Enable

ĈĒ ₁	CE ₂	CS	(CS*) ^[2]	8185 Status
1	Х	×	0	Power Down and Function Disable[1]
х	0	х	0	Power Down and Function Disable[1]
0	1	1	0	Powered Up and Function Disable[1]
0	1	0	1	Powered Up and Enabled

NOTES:

- X: Don't Care.
- Function Disable implies Data Bus in high impedance state and not writing.
- 2: $CS^* = (\overline{CE}_1 = \overline{0}) \cdot (CE_2 = 1) \cdot (\overline{CS} = 0)$
 - CS* = 1 signifies all chip enables and chip select active

Table 2.
Truth Table for
Control and Data Bus Pin Status

(CS*)	RD	WR	AD ₀₋₇ During Data Portion of Cycle	8185 Function
0	Х	Х	Hi-Impedance	No Function
1	0	1	Data from Memory	Read
1	1	0	Data to Memory	Write
1	1	1	Hi-Impedance	Reading, but not Driving Data Bus

NOTE:

X: Don't Care.

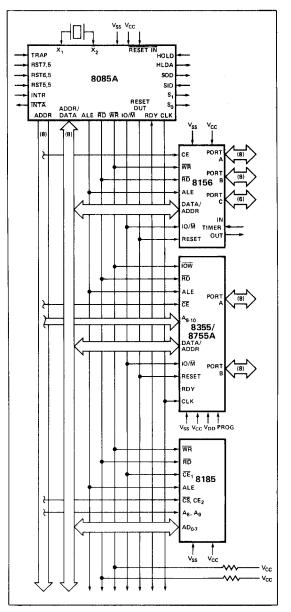


Figure 3. 8185 in an MCS-85 System

- 4 Chips:
- 2K Bytes ROM
- 1.25K Bytes RAM
- 38 I/O Lines
- 1 Counter/Timer
- 2 Serial I/O Lines 5 Interrupt Inputs

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IAPX 88 FIVE CHIP SYSTEM:

- 1.25 K Bytes RAM
- 2 K Bytes ROM
- 38 I/O Pins
- 1 Internal Timer
- 2 Interrupt Levels

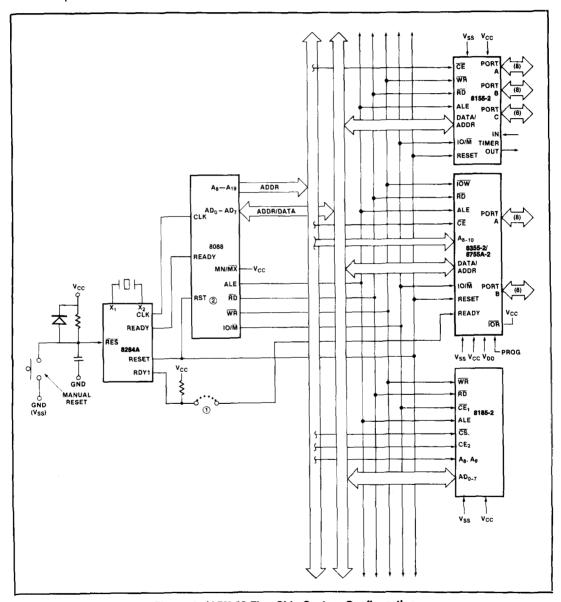


Figure 4. iAPX 88 Five Chip System Configuration



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	. 0°C to +70°C
Storage Temperature	65°C to +150°C
Voltage on Any Pin	
with Respect to Ground	0.5V to +7V
Power Dissipation	1.5W

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS $(T_A = 0^{\circ}C \text{ to } 70^{\circ}C, V_{CC} = 5V \pm 5\%)$

Symbol	Parameter	Min.	Max.	Units	Test Conditions
VIL	Input Low Voltage	-0.5	0.8	٧	
ViH	Input High Voltage	2.0	V _{CC} +0.5	٧	
VoL	Output Low Voltage		0.45	V	IOL = 2mA
Voн	Output High Voltage	2.4			$I_{OH} = -400\mu A$
lıL	Input Leakage		±10	μΑ	0V ≤V _{IN} ≤V _{CC}
ILO	Output Leakage Current		±10	μА	0.45V ≤ V _{OUT} ≤ V _{CC}
Icc	Vcc Supply Current Powered Up		100	mA	
	Powered Down		35	mA	

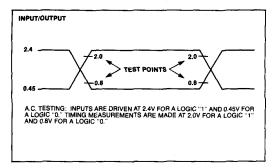
A.C. CHARACTERISTICS $(T_A = 0^{\circ}C \text{ to } 70^{\circ}C, V_{CC} = 5V \pm 5\%)$

		8185		8185-2		
Symbol	Parameter	Min.	Max.	Min.	Max.	Units
tal	Address to Latch Set Up Time	50		30		ns
tLA	Address Hold Time After Latch	80		30		ns
tLC	Latch to READ/WRITE Control	100		40		ns
tRD	Valid Data Out Delay from READ Control		170		140	ns
tLD	ALE to Data Out Valid		300		200	ns
tLL	Latch Enable Width	100		70		ns
tRDF	Data Bus Float After READ	0	100	0	80	ns
tcL	READ/WRITE Control to Latch Enable	20		10		ns
tcc	READ/WRITE Control Width	250		200		ns
tow	Data In to WRITE Set Up Time	150		150		ns
two	Data In Hold Time After WRITE	20		20		ns
tsc	Chip Select Set Up to Control Line	10		10		ns
tcs	Chip Select Hold Time After Control	10		10		ns
tALCE	Chip Enable Set Up to ALE Falling	30		10		ns
tLACE	Chip Enable Hold Time After ALE	50		30		ns

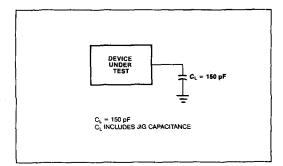
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A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT



WAVEFORM

