# 28F008SA
# 8-MBIT (1-MBIT x 8) FLASHFILE™ MEMORY

- **High-Density Symmetrically Blocked Architecture**
  - **Sixteen 64-Kbyte Blocks**
- **Extended Cycling Capability**
  - **100,000 Block Erase Cycles**
  - **1.6 Million Block Erase Cycles per Chip**
- **Automated Byte Write and Block Erase**
  - **Command User Interface**
  - **Status Register**
- **System Performance Enhancements**
  - **RY/BY# Status Output**
  - **Erase Suspend Capability**
- **Deep-Powerdown Mode**
  - **0.20 μA $I_{CC}$ Typical**
- **Very High-Performance Read**
  - **85 ns Maximum Access Time**
- **SRAM-Compatible Write Interface**
- **Hardware Data Protection Feature**
  - **Erase/Write Lockout during Power Transitions**
- **Industry Standard Packaging**
  - **40-Lead TSOP, 44-Lead PSOP**
- **ETOX III Nonvolatile Flash Technology**
  - **12V Byte Write/Block Erase**
- **Independent Software Vendor Support**
  - **Microsoft* Flash File System (FFS)**

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Intel's 28F008SA 8-Mbit FlashFile™ Memory is the highest density nonvolatile read/write solution for solid state storage. The 28F008SA's extended cycling, symmetrically blocked architecture, fast access time, write automation and low power consumption provide a more reliable, lower power, lighter weight and higher performance alternative to traditional rotating disk technology. The 28F008SA brings new capabilities to portable computing. Application and operating system software stored in resident flash memory arrays provide instant-on, rapid execute-in-place and protection from obsolescence through in-system software updates. Resident software also extends system battery life and increases reliability by reducing disk drive accesses.

For high density data acquisition applications, the 28F008SA offers a more cost-effective and reliable alternative to SRAM and battery. Traditional high density embedded applications, such as telecommunications, can take advantage of the 28F008SA's nonvolatility, blocking and minimal system code requirements for flexible firmware and modular software designs.

The 28F008SA is offered in 40-lead TSOP (standard and reverse) and 44-lead PSOP packages. Pin assignments simplify board layout when integrating multiple devices in a flash memory array or subsystem. This device uses an integrated Command User Interface and state machine for simplified block erasure and byte write. The 28F008SA memory map consists of 16 separately erasable 64-Kbyte blocks.

Intel's 28F008SA employs advanced CMOS circuitry for systems requiring low power consumption and noise immunity. Its 85 ns access time provides superior performance when compared with magnetic storage media. A deep powerdown mode lowers power consumption to 1 μW typical thru $V_{CC}$, crucial in portable computing, handheld instrumentation and other low-power applications. The RP# power control input also provides absolute data protection during system powerup/down.

Manufactured on Intel's 0.8 micron ETOX process, the 28F008SA provides the highest levels of quality, reliability and cost-effectiveness.

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*Microsoft is a trademark of Microsoft Corporation.

October 1993
Order Number: 290429-004

## PRODUCT OVERVIEW

The 28F008SA is a high-performance **8-Mbit** (8,388,608 bit) memory organized as **1 Mbyte** (1,048,576 bytes) of 8 bits each. **Sixteen 64-Kbyte** (65,536 byte) **blocks** are included on the 28F008SA. A memory map is shown in Figure 6 of this specification. A block erase operation erases one of the sixteen blocks of memory in typically **1.6 seconds**, independent of the remaining blocks. Each block can be independently erased and written **100,000 cycles**. **Erase Suspend** mode allows system software to suspend block erase to read data or execute code from any other block of the 28F008SA.

The 28F008SA is available in the **40-lead TSOP** (Thin Small Outline Package, 1.2 mm thick) and **44-lead PSOP** (Plastic Small Outline) packages. Pinouts are shown in Figures 2 and 4 of this specification.

The **Command User Interface** serves as the interface between the microprocessor or microcontroller and the internal operation of the 28F008SA.

**Byte Write and Block Erase Automation** allow byte write and block erase operations to be executed using a two-write command sequence to the Command User Interface. The internal **Write State Machine** (WSM) automatically executes the algorithms and timings necessary for byte write and block erase operations, including verifications, thereby unburdening the microprocessor or microcontroller. Writing of memory data is performed in byte increments typically within **9 µs**, an 80% improvement over current flash memory products. **$I_{PP}$ byte write and block erase currents** are **10 mA typical, 30 mA maximum. $V_{PP}$ byte write and block erase voltage** is **11.4V to 12.6V**.

The **Status Register** indicates the status of the WSM and when the WSM successfully completes the desired byte write or block erase operation.

The **RY/BY#** output gives an additional indicator of WSM activity, providing capability for both hardware signal of status (versus software polling) and status masking (interrupt masking for background erase, for example). Status polling using RY/BY# minimizes both CPU overhead and system power consumption. When low, RY/BY# indicates that the WSM is performing a block erase or byte write operation. RY/BY# high indicates that the WSM is ready for new commands, block erase is suspended or the device is in deep powerdown mode.

Maximum access time is **85 ns ($t_{ACC}$)** over the commercial temperature range (0°C to +70°C) and over $V_{CC}$ supply voltage range (4.5V to 5.5V and 4.75V to 5.25V). **$I_{CC}$ active current** (CMOS Read) is **20 mA typical, 35 mA maximum at 8 MHz**.

When the CE# and RP# pins are at $V_{CC}$, the **$I_{CC}$ CMOS Standby** mode is enabled.

A **Deep Powerdown** mode is enabled when the RP# pin is at GND, minimizing power consumption and providing write protection. **$I_{CC}$ current** in deep powerdown is **0.20 µA typical**. Reset time of 400 ns is required from RP# switching high until outputs are valid to read attempts. Equivalently, the device has a wake time of 1 µs from RP# high until writes to the Command User Interface are recognized by the 28F008SA. With RP# at GND, the WSM is reset and the Status Register is cleared.

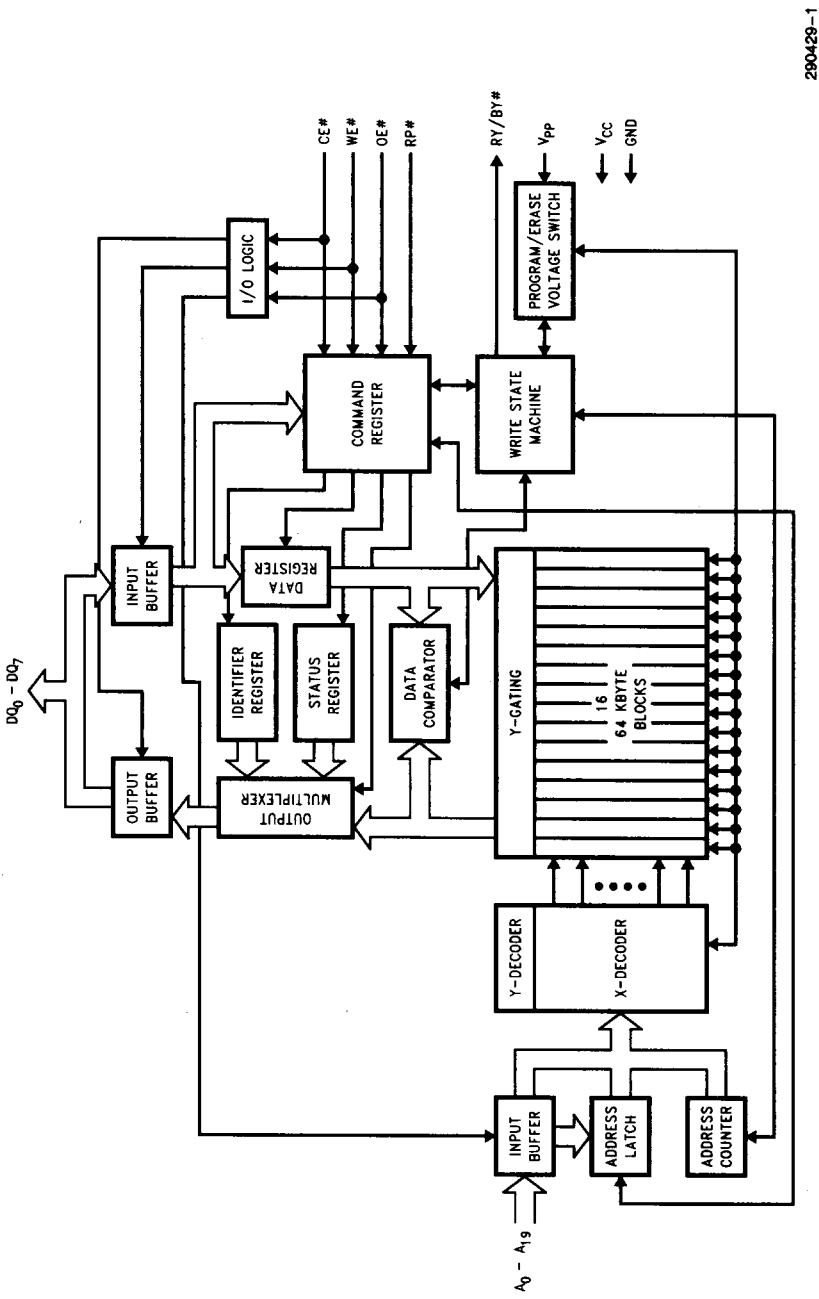


**Figure 1. Block Diagram**

**Table 1. Pin Description**

| Symbol | Type | Name and Function |
|---|---|---|
| $A_0$–$A_{19}$ | INPUT | **ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle. |
| $DQ_0$–$DQ_7$ | INPUT/OUTPUT | **DATA INPUT/OUTPUTS:** Inputs data and commands during Command User Interface write cycles; outputs data during memory array, Status Register and Identifier read cycles. The data pins are active high and float to tri-state off when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle. |
| CE# | INPUT | **CHIP ENABLE:** Activates the device's control logic, input buffers, decoders, and sense amplifiers. CE# is active low; CE# high deselects the memory device and reduces power consumption to standby levels. |
| RP# | INPUT | **RESET/DEEP POWERDOWN:** Puts the device in deep powerdown mode. RP# is active low; RP# high gates normal operation. RP# also locks out block erase or byte write operations when active low, providing data protection during power transitions. RP# active resets internal automation. Exit from Deep Powerdown sets device to read-array mode. |
| OE# | INPUT | **OUTPUT ENABLE:** Gates the device's outputs through the data buffers during a read cycle. OE# is active low. |
| WE# | INPUT | **WRITE ENABLE:** Controls writes to the Command User Interface and array blocks. WE# is active low. Addresses and data are latched on the rising edge of the WE# pulse. |
| RY/BY# | OUTPUT | **READY/BUSY#:** Indicates the status of the internal Write State Machine. When low, it indicates that the WSM is performing a block erase or byte write operation. RY/BY# high indicates that the WSM is ready for new commands, block erase is suspended or the device is in deep powerdown mode. RY/BY# is always active and does **NOT** float to tri-state off when the chip is deselected or data outputs are disabled. |
| $V_{PP}$ | | **BLOCK ERASE/BYTE WRITE POWER SUPPLY** for erasing blocks of the array or writing bytes of each block.<br>**NOTE:**<br>With $V_{PP} < V_{PPLMAX}$, memory contents cannot be altered. |
| $V_{CC}$ | | **DEVICE POWER SUPPLY (5V ± 10%, 5V ± 5%)** |
| GND | | **GROUND** |

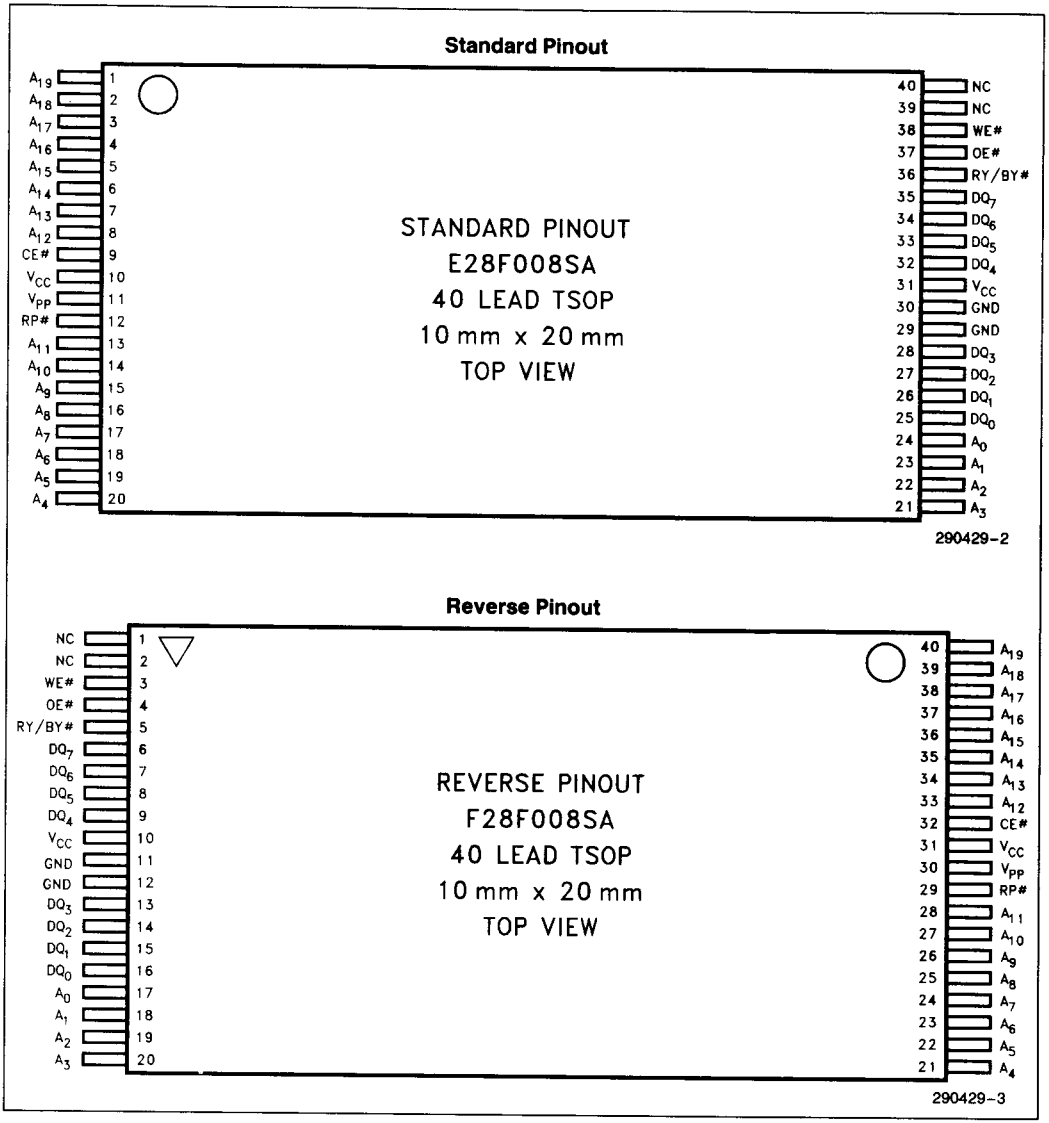


**Figure 2. TSOP Lead Configurations**

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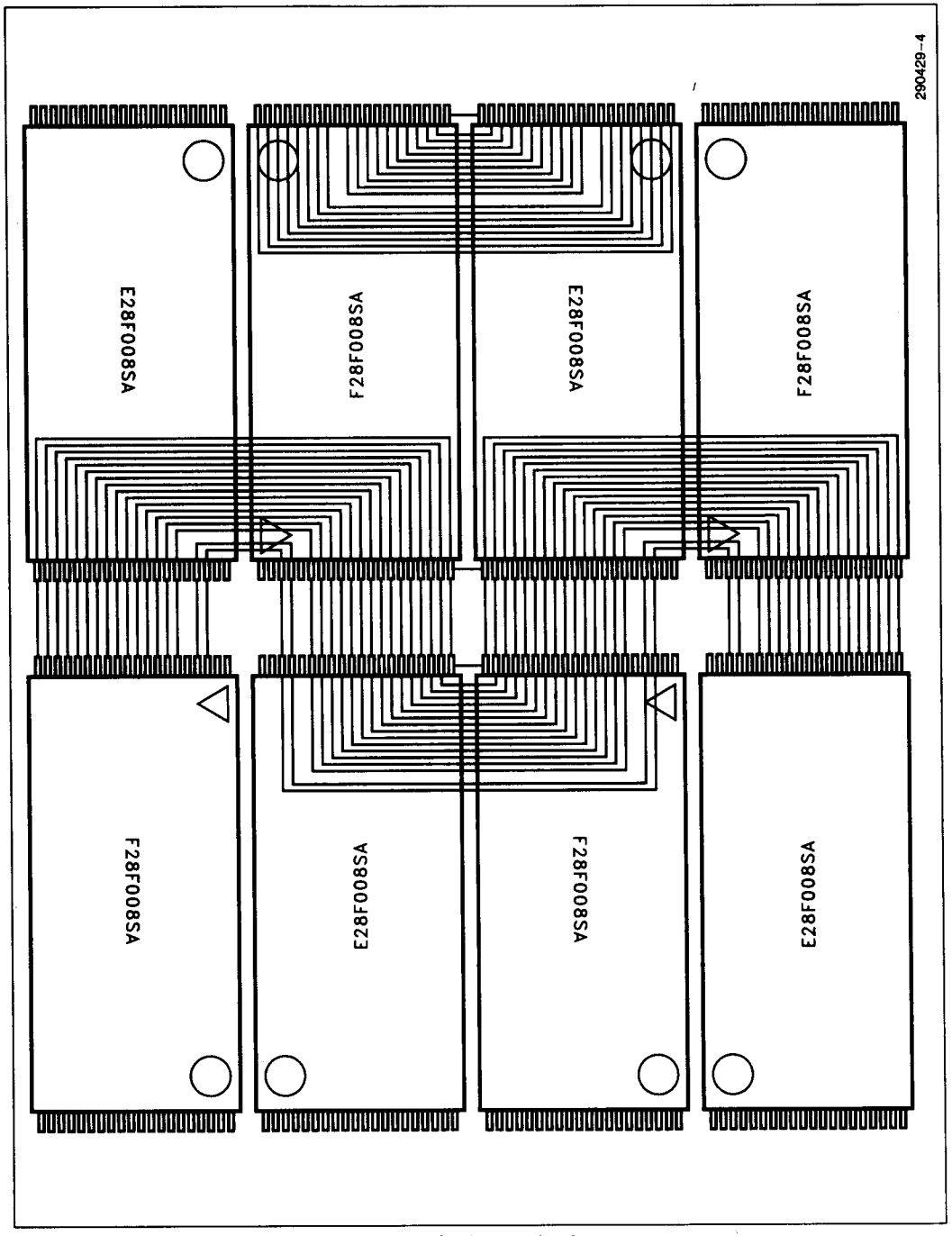


**Figure 3. TSOP Serpentine Layout**

**NOTE:**
1. Connect all $V_{CC}$ and GND pins of each device to common power supply outputs. DO NOT leave $V_{CC}$ or GND inputs disconnected.

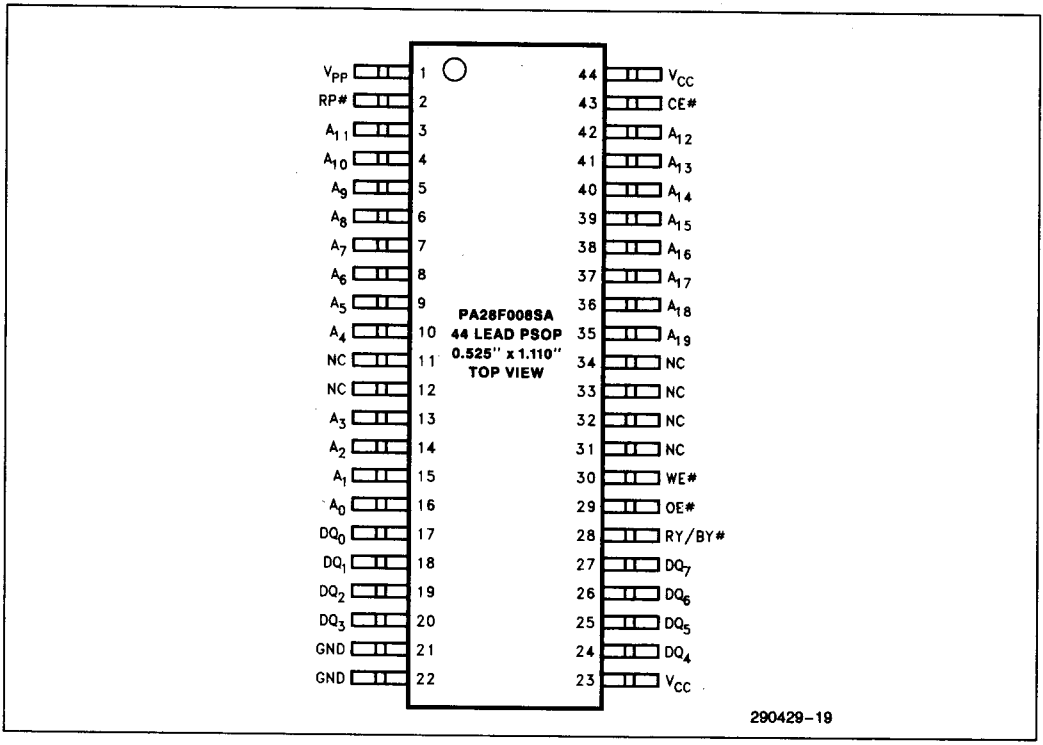


**Figure 4. PSOP Lead Configuration**

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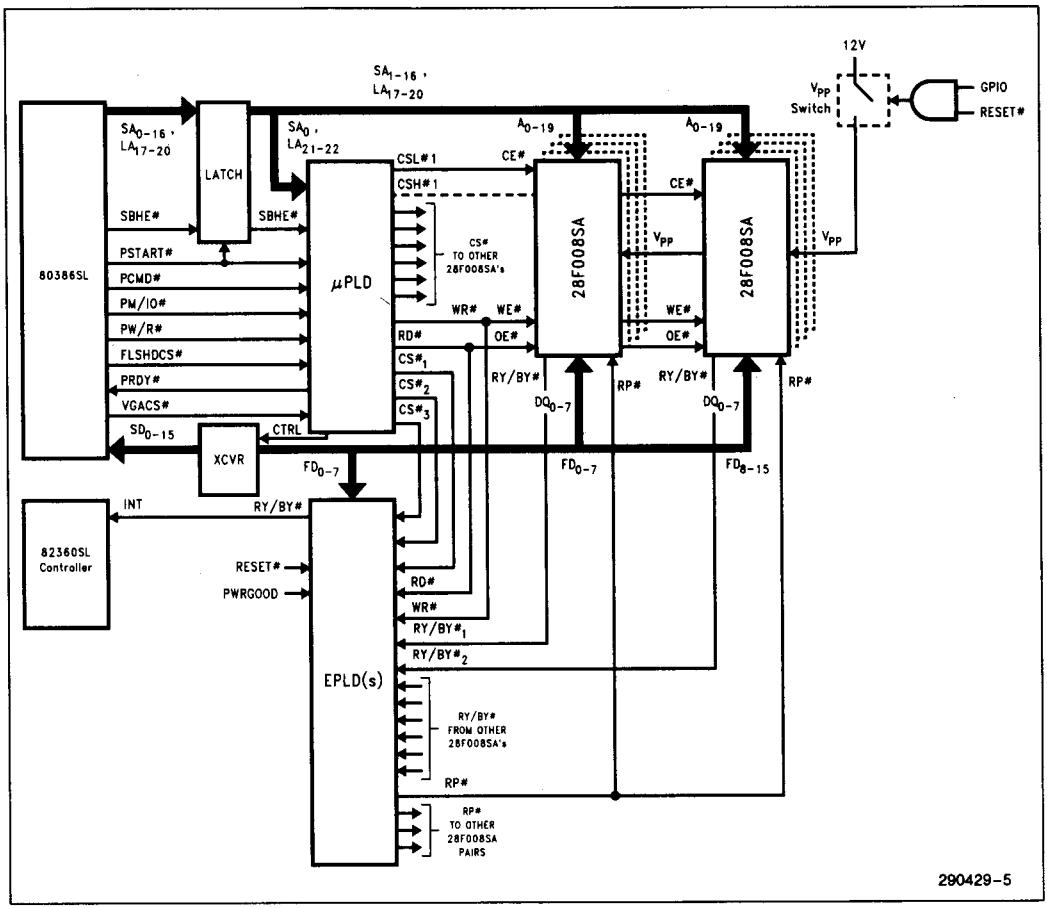


**Figure 5. 28F008SA Array Interface to Intel386SL Microprocessor Superset through PI Bus (Including RY/BY# Masking and Selective Powerdown), for DRAM Backup during System SUSPEND, Resident O/S and Applications and Motherboard Solid-State Disk.**

## PRINCIPLES OF OPERATION

The 28F008SA includes on-chip write automation to manage write and erase functions. The Write State Machine allows for: 100% TTL-level control inputs; fixed power supplies during block erasure and byte write; and minimal processor overhead with RAM-like interface timings.

After initial device powerup, or after return from deep powerdown mode (see Bus Operations), the 28F008SA functions as a read-only memory. Manipulation of external memory-control pins allow array read, standby and output disable operations. Both Status Register and intelligent identifiers can also be accessed through the Command User Interface when $V_{PP} = V_{PPL}$.

This same subset of operations is also available when high voltage is applied to the $V_{PP}$ pin. In addition, high voltage on $V_{PP}$ enables successful block erasure and byte writing of the device. All functions associated with altering memory contents—byte write, block erase, status and intelligent identifier—are accessed via the Command User Interface and verified thru the Status Register.

Commands are written using standard microprocessor write timings. Command User Interface contents serve as input to the WSM, which controls the block erase and byte write circuitry. Write cycles also internally latch addresses and data needed for byte write or block erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the intelligent identifier codes, or output byte write and block erase status for verification.

Interface software to initiate and poll progress of internal byte write and block erase can be stored in any of the 28F008SA blocks. This code is copied to, and executed from, system RAM during actual flash memory update. After successful completion of byte write and/or block erase, code/data reads from the 28F008SA are again possible via the Read Array command. Erase suspend/resume capability allows system software to suspend block erase to read data and execute code from any other block.

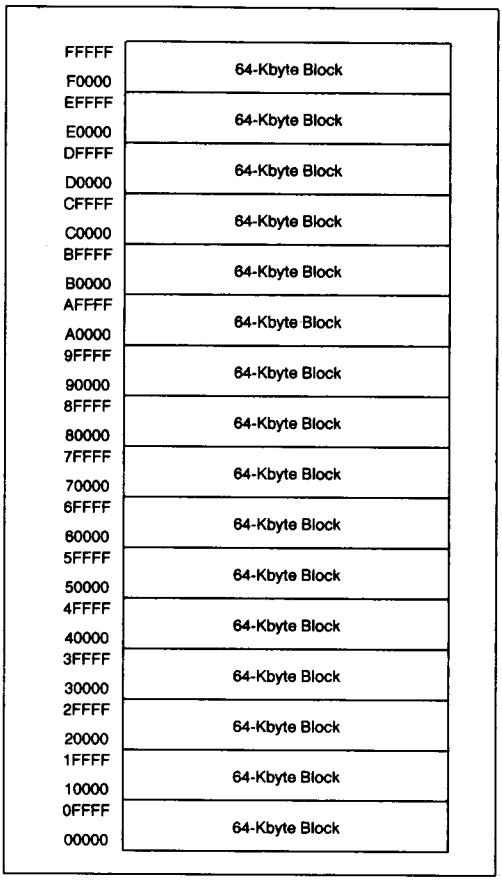


**Figure 6. Memory Map**

## Command User Interface and Write Automation

An on-chip state machine controls block erase and byte write, freeing the system processor for other tasks. After receiving the Erase Setup and Erase Confirm commands, the state machine controls block pre-conditioning and erase, returning progress via the Status Register and RY/BY# output. Byte write is similarly controlled, after destination address and expected data are supplied. The program and erase algorithms of past Intel flash memories are now regulated by the state machine, including pulse repetition where required and internal verification and margining of data.

## Data Protection

Depending on the application, the system designer may choose to make the $V_{PP}$ power supply switchable (available only when memory byte writes/block erases are required) or hardwired to $V_{PPH}$. When $V_{PP} = V_{PPL}$, memory contents cannot be altered. The 28F008SA Command User Interface architecture provides protection from unwanted byte write or block erase operations even when high voltage is applied to $V_{PP}$. Additionally, all functions are disabled whenever $V_{CC}$ is below the write lockout voltage $V_{LKO}$, or when RP# is at $V_{IL}$. The 28F008SA accommodates either design practice and encourages optimization of the processor-memory interface.

The two-step byte write/block erase Command User Interface write sequence provides additional software write protection.

## BUS OPERATION

Flash memory reads, erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

## Read

The 28F008SA has three read modes. The memory can be read from any of its blocks, and information can be read from the intelligent identifier or Status Register. $V_{PP}$ can be at either $V_{PPL}$ or $V_{PPH}$.

The first task is to write the appropriate read mode command to the Command User Interface (array, intelligent identifier, or Status Register). The 28F008SA automatically resets to Read Array mode upon initial device powerup or after exit from deep powerdown. The 28F008SA has four control pins, two of which must be logically active to obtain data at the outputs. Chip Enable (CE#) is the device selection control, and when active enables the selected memory device. Output Enable (OE#) is the data input/output ($DQ_0$–$DQ_7$) direction control, and when active drives data from the selected memory onto the I/O bus. RP# and WE# must also be at $V_{IH}$. Figure 10 illustrates read bus cycle waveforms.

## Output Disable

With OE# at a logic-high level ($V_{IH}$), the device outputs are disabled. Output pins ($DQ_0$–$DQ_7$) are placed in a high-impedance state.

## Standby

CE# at a logic-high level ($V_{IH}$) places the 28F008SA in standby mode. Standby operation disables much of the 28F008SA's circuitry and substantially reduces device power consumption. The outputs ($DQ_0$–$DQ_7$) are placed in a high-impedence state independent of the status of OE#. If the 28F008SA is deselected during block erase or byte write, the device will continue functioning and consuming normal active power until the operation completes.

**Table 2. Bus Operations**

| Mode | Notes | RP# | CE# | OE# | WE# | $A_0$ | $V_{PP}$ | $DQ_{0-7}$ | RY/BY# |
|---|---|---|---|---|---|---|---|---|---|
| Read | 1, 2, 3 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | X | $D_{OUT}$ | X |
| Output Disable | 3 | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | X | High Z | X |
| Standby | 3 | $V_{IH}$ | $V_{IH}$ | X | X | X | X | High Z | X |
| Deep PowerDown | | $V_{IL}$ | X | X | X | X | X | High Z | $V_{OH}$ |
| Intelligent Identifier (Mfr) | | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | 89H | $V_{OH}$ |
| Intelligent Identifier (Device) | | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | A2H | $V_{OH}$ |
| Write | 3, 4, 5 | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | X | $D_{IN}$ | X |

**NOTES:**
1. Refer to DC Characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. X can be $V_{IL}$ or $V_{IH}$ for control pins and addresses, and $V_{PPL}$ or $V_{PPH}$ for $V_{PP}$. See DC Characteristics for $V_{PPL}$ and $V_{PPH}$ voltages.
3. RY/BY# is $V_{OL}$ when the Write State Machine is executing internal block erase or byte write algorithms. It is $V_{OH}$ when the WSM is not busy, in Erase Suspend mode or deep powerdown mode.
4. Command writes involving block erase or byte write are only successfully executed when $V_{PP} = V_{PPH}$.
5. Refer to Table 3 for valid $D_{IN}$ during a write operation.

## Deep Power-Down

The 28F008SA offers a deep power-down feature, entered when RP# is at $V_{IL}$. Current draw thru $V_{CC}$ is 0.20 μA typical in deep power-down mode, with current draw through $V_{PP}$ typically 0.1 μA. During read modes, RP#-low deselects the memory, places output drivers in a high-impedence state and turns off all internal circuits. The 28F008SA requires time $t_{PHQV}$ (see AC Characteristics-Read-Only Operations) after return from powerdown until initial memory access outputs are valid. After this wakeup interval, normal operation is restored. The Command User Interface is reset to Read Array, and the upper 5 bits of the Status Register are cleared to value 10000, upon return to normal operation.

During block erase or byte write modes, RP# low will abort either operation. Memory contents of the block being altered are no longer valid as the data will be partially written or erased. Time $t_{PHWL}$ after RP# goes to logic-high ($V_{IH}$) is required before another command can be written.

This use of RP# during system reset is important with automated write/erase devices. When the system comes out of reset it expects to read from the flash memory. Automated flash memories provide status information when accessed during write/erase modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization would not occur because the flash memory would be providing the status information instead of array data. Intel's Flash Memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application RP# is controlled by the same RESET# signal that resets the system CPU.

## Intelligent Identifier Operation

The intelligent identifier operation outputs the manufacturer code, 89H; and the device code, A2H for the 28F008SA. The system CPU can then automatically match the device with its proper block erase and byte write algorithms.

The manufacturer- and device-codes are read via the Command User Interface. Following a write of 90H to the Command User Interface, a read from address location 00000H outputs the manufacturer code (89H). A read from address 00001H outputs the device code (A2H). It is not necessary to have high voltage applied to $V_{PP}$ to read the intelligent identifiers from the Command User Interface.

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**Table 3. Command Definitions**

| Command | Bus Cycles Req'd | Notes | First Bus Cycle | | | Second Bus Cycle | | |
|---|---|---|---|---|---|---|---|---|
| | | | Operation | Address | Data | Operation | Address | Data |
| Read Array/Reset | 1 | 1 | Write | X | FFH | | | |
| Intelligent Identifier | 3 | 2, 3, 4 | Write | X | 90H | Read | IA | IID |
| Read Status Register | 2 | 3 | Write | X | 70H | Read | X | SRD |
| Clear Status Register | 1 | | Write | X | 50H | | | |
| Erase Setup/Erase Confirm | 2 | 2 | Write | BA | 20H | Write | BA | D0H |
| Erase Suspend/Erase Resume | 2 | | Write | X | B0H | Write | X | D0H |
| Byte Write Setup/Write | 2 | 2, 3, 5 | Write | WA | 40H | Write | WA | WD |
| Alternate Byte Write Setup/Write | 2 | 2, 3, 5 | Write | WA | 10H | Write | WA | WD |

**NOTES:**
1. Bus operations are defined in Table 2.
2. IA = Identifier Address: 00H for manufacturer code, 01H for device code.
   BA = Address within the block being erased.
   WA = Address of memory location to be written.
3. SRD = Data read from Status Register. See Table 4 for a description of the Status Register bits.
   WD = Data to be written at location WA. Data is latched on the rising edge of WE#.
   IID = Data read from Intelligent Identifiers.
4. Following the Intelligent Identifier command, two read operations access manufacture and device codes.
5. Either 40H or 10H are recognized by the WSM as the Byte Write Setup command.
6. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.