



8216/8226 4-BIT PARALLEL BIDIRECTIONAL BUS DRIVER

- Data Bus Buffer Driver for 8080 CPU
 - Low Input Load Current — 0.25 mA Maximum
 - High Output Drive Capability for Driving System Bus
- 3.65V Output High Voltage for Direct Interface to 8080 CPU
 - 3-State Outputs
 - Reduces System Package Count

The 8216/8226 is a 4-bit bidirectional bus driver/receiver. All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V V_{OH} , and for high capacitance terminated bus structures, the DB outputs provide a high 50 mA I_{OL} capability. A non-inverting (8216) and an inverting (8226) are available to meet a wide variety of applications for buffering in microcomputer systems.

*Note: The specifications for the 3216/3226 are identical with those for the 8216/8226.

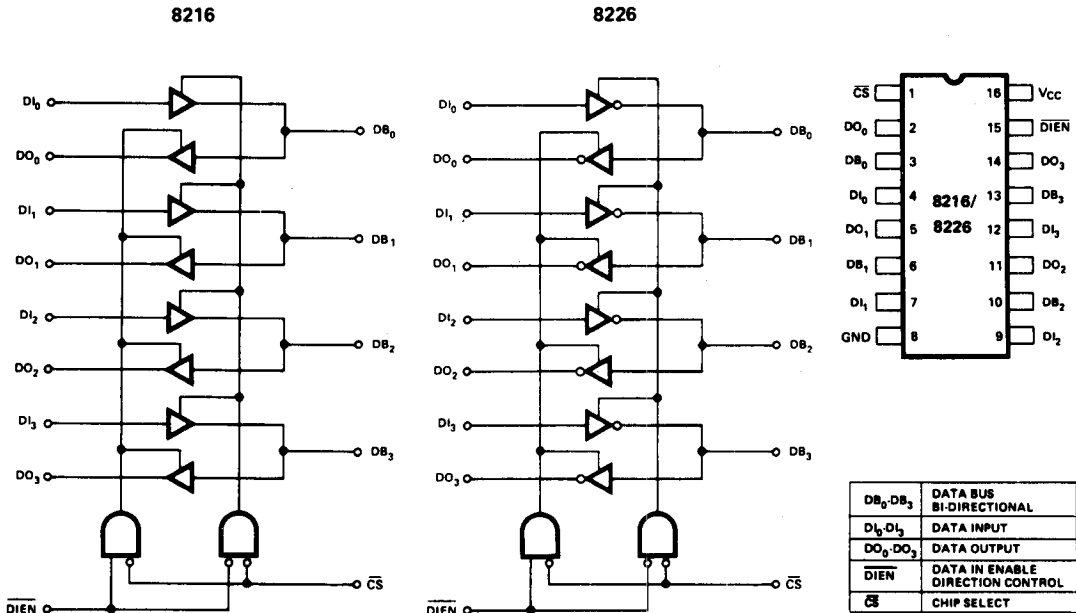


Figure 1. Block Diagrams

Figure 2. Pin Configuration

FUNCTIONAL DESCRIPTION

Microprocessors like the 8080 are MOS devices and are generally capable of driving a single TTL load. The same is true for MOS memory devices. While this type of drive is sufficient in small systems with few components, quite often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multi-board system.

The 8216/8226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bidirectional Driver

Each buffered line of the four bit driver consists of two separate buffers that are tri-state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is direct TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus such as the 8080 Data Bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65V) so that direct interface to the 8080 and 8008 CPUs is achieved with an adequate amount of noise immunity (350mV worst case).

Control Gating \overline{DIEN} , \overline{CS}

The \overline{CS} input is actually a device select. When it is "high" the output drivers are all forced to their high-impedance state. When it is at "zero" the device is selected (enabled) and the direction of the data flow is determined by the \overline{DIEN} input.

The \overline{DIEN} input controls the direction of data flow (see Figure 3) for complete truth table. This direction control is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

The 8216/8226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.

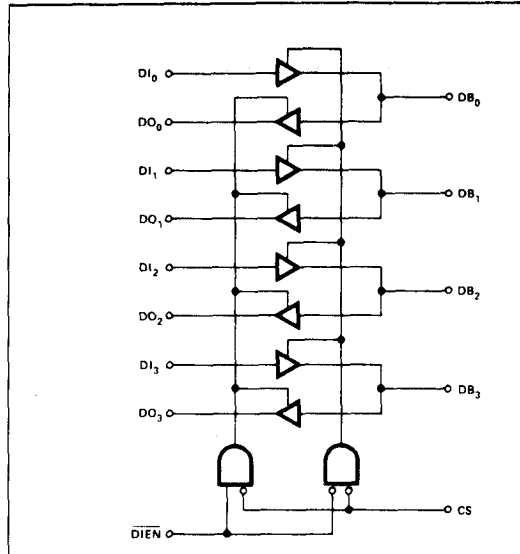


Figure 3a. 8216 Logic Diagram

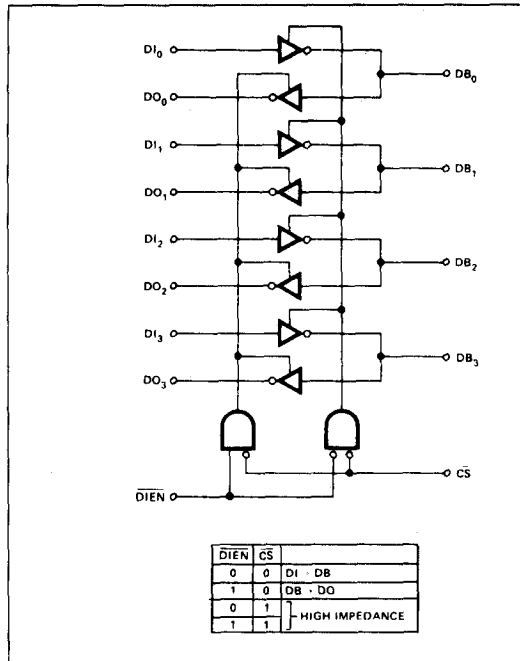


Figure 3b. 8226 Logic Diagram

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Currents	125 mA

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$)

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.	Max.		
I_{F1}	Input Load Current \overline{DIEN} , \overline{CS}		-0.15	-5	mA	$V_F = 0.45$
I_{F2}	Input Load Current All Other Inputs		-0.08	-25	mA	$V_F = 0.45$
I_{R1}	Input Leakage Current \overline{DIEN} , \overline{CS}			80	μA	$V_R = 5.25\text{V}$
I_{R2}	Input Leakage Current DI Inputs			40	μA	$V_R = 5.25\text{V}$
V_C	Input Forward Voltage Clamp			-1	V	$I_C = -5\text{mA}$
V_{IL}	Input "Low" Voltage			.95	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{O1}	Output Leakage Current (3-State)			20 100	μA	$V_O = 0.45\text{V}/5.25\text{V}$
I_{CC}	Power Supply Current	8216	95	130	mA	
		8226	85	120	mA	
V_{OL1}	Output "Low" Voltage		0.3	.45	V	DO Outputs $I_{OL} = 15\text{mA}$ DB Outputs $I_{OL} = 25\text{mA}$
V_{OL2}	Output "Low" Voltage	8216	0.5	.6	V	DB Outputs $I_{OL} = 55\text{mA}$
		8226	0.5	.6	V	DB Outputs $I_{OL} = 50\text{mA}$
V_{OH1}	Output "High" Voltage	3.65	4.0		V	DO Outputs $I_{OH} = -1\text{mA}$
V_{OH2}	Output "High" Voltage	2.4	3.0		V	DB Outputs $I_{OH} = -10\text{mA}$
I_{OS}	Output Short Circuit Current		-15	-35	mA	DO Outputs $V_O \cong 0\text{V}$,
			-30	-75	mA	DB Outputs $V_{CC} = 5.0\text{V}$

NOTE:

Typical values are for $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$.

CAPACITANCE^[6] ($V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25^\circ C$, $f = 1\text{ MHz}$)

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
C _{IN}	Input Capacitance		4	8	pF
C _{OUT1}	Output Capacitance		6	10	pF
C _{OUT2}	Output Capacitance		13	18	pF

A.C. CHARACTERISTICS ($T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = +5V \pm 5\%$)

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
T _{PD1}	Input to Output Delay DO Outputs		15	25	ns	C _L =30pF, R ₁ =300Ω R ₂ =600Ω
T _{PD2}	Input to Output Delay DB Outputs 8216		19	30	ns	C _L =300pF, R ₁ =90Ω R ₂ =180Ω
			16	25	ns	
T _E	Output Enable Time 8216		42	65	ns	(Note 2)
			36	54	ns	(Note 3)
T _D	Output Disable Time		16	35	ns	(Note 4)

NOTE:

Input pulse amplitude of 2.5V.

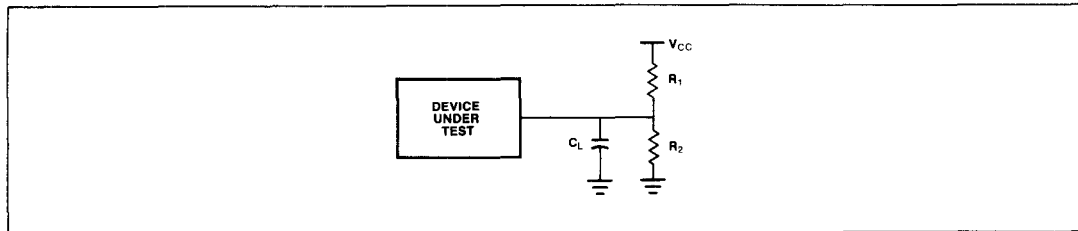
Input rise and fall times of 5 ns between 1 and 2 volts.

Output loading is 5 mA and 10 pF.

Speed measurements are made at 1.5 volt levels.

NOTES:

1. Typical values are for $T_A = 25^\circ C$, $V_{CC} = 5.0V$.
2. DO Outputs, C_L = 30pF, R₁ = 300/10 KΩ, R₂ = 180/1KΩ; DB Outputs, C_L = 300pF, R₁ = 90/10 KΩ, R₂ = 180/1 KΩ.
3. DO Outputs, C_L = 30pF, R₁ = 300/10 KΩ, R₂ = 600/1K; DB Outputs, C_L = 300pF, R₁ = 90/10 KΩ, R₂ = 180/1 KΩ.
4. DO Outputs, C_L = 5pF, R₁ = 300/10 KΩ, R₂ = 600/1 KΩ; DB Outputs, C_L = 5pF, R₁ = 90/10 KΩ, R₂ = 180/1 KΩ.
5. This parameter is periodically sampled and not 100% tested.

A.C. TESTING LOAD CIRCUIT


WAVEFORM

