

NEC Microcomputers, Inc.

μ PB8214

PRIORITY INTERRUPT CONTROLLER

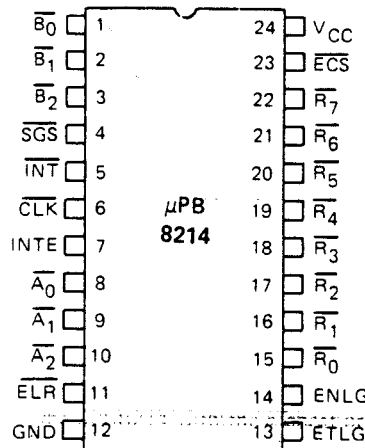
DESCRIPTION The μ PB8214 is an eight-level priority interrupt controller. Designed to simplify interrupt driven microcomputer systems, the μ PB8214 requires a single +5V power supply and is packaged in a 24 pin plastic Dual-in-line package.

The μ PB8214 accepts up to eight interrupts, determines which has the highest priority and then compares that priority with a software created current status register. If the incoming requires is of a higher priority than the interrupt currently being serviced, an interrupt request to the processor is generated. Vector information that identifies the interrupting device is also generated.

The interrupt structure of the microcomputer system can be expanded beyond eight interrupt levels by cascading μ PB8214s. The μ PB8214's interrupt and vector information outputs are open collector and control signals are provided to simplify expansion of the interrupt structure.

- FEATURES**
- Eight Priority Levels
 - Current Status Register and Priority Comparator
 - Easily Expanded Interrupt Structure
 - Single +5 Volt Supply

PIN CONFIGURATION

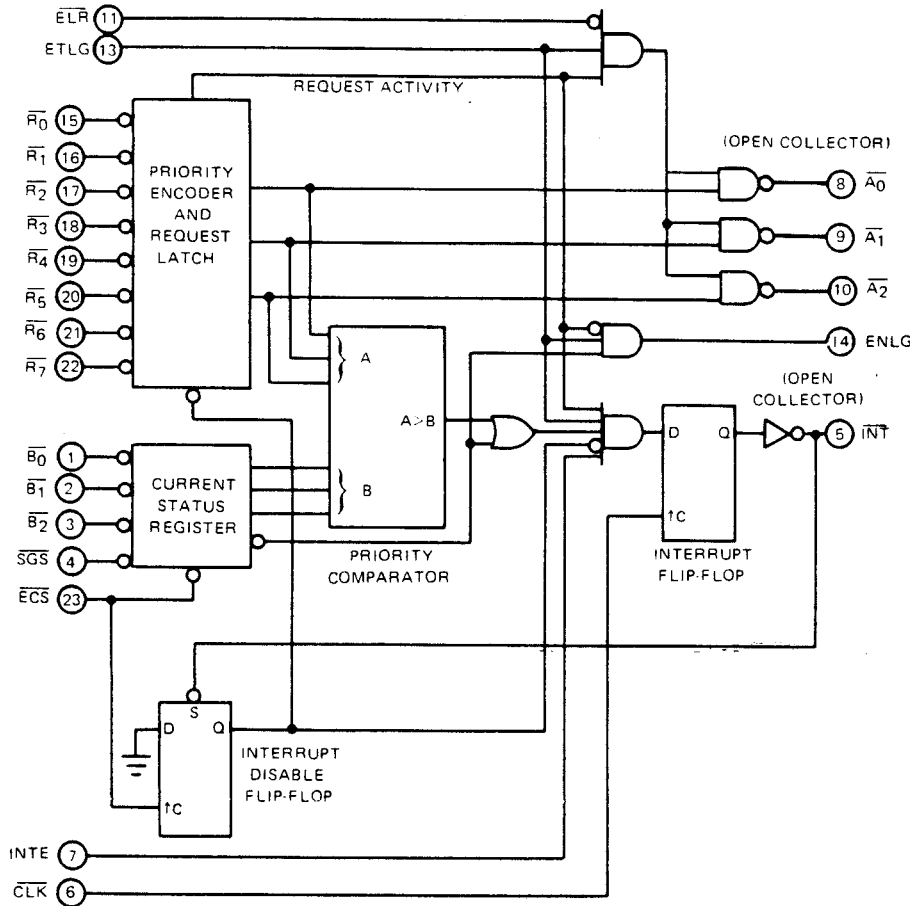


PIN NAMES

Inputs		
\overline{R}_0 - \overline{R}_7	Request Levels (\overline{R}_7 Highest Priority)	
\overline{B}_0 - \overline{B}_2	Current Status	
SGS	Status Group Select	
ECS	Enable Current Status	
INTE	Interrupt Enable	
\overline{CLK}	Clock (INT F F1)	
ELR	Enable Level Reset	
ETLG	Enable This Level Group	
Outputs		
\overline{A}_0 - \overline{A}_2	Request Levels	Open Collector
INT	Interrupt (Act. Low)	Collector
ENLG	Enable Next Level Group	

μPB8214

BLOCK DIAGRAM



General

The μPB8214 is an LSI device designed to simplify the circuitry required to implement an interrupt driven microcomputer system. Up to eight interrupting devices can be connected to a μPB8214, which will assign priority to incoming interrupt requests and accept the highest. It will also compare the priority of the highest incoming request with the priority of the interrupt being serviced. If the serviced interrupt has a higher priority, the incoming request will not be accepted.

A system with more than eight interrupting devices can be implemented by interconnecting additional μPB8214s. In order to facilitate this expansion, control signals are provided for cascading the controllers so that there is a priority established among the controllers. In addition, the interrupt and vector information outputs are open collector.

Priority Encoder and Request Latch

The priority encoder portion of the μPB8214 accepts up to eight active low interrupt requests (\bar{R}_0 – \bar{R}_7). The circuit assigns priority to the incoming requests, with \bar{R}_7 having the highest priority and \bar{R}_0 the lowest. If two or more requests occur simultaneously, the μPB8214 accepts the one having the highest priority. Once an incoming interrupt request is accepted, it is stored by the request latch and a three-bit code is output. As shown in the following table, the outputs, (\bar{A}_0 – \bar{A}_2) are the complement of the request level (modulo 8) and directly correspond to the bit pattern required to generate the one byte RESTART (RST) instructions recognized by an 8080A. Simultaneously with the \bar{A}_0 – \bar{A}_2 outputs, a system interrupt request (\bar{INT}) is output by the μPB8214. It should be noted that incoming interrupt requests that are *not* accepted are not latched and must remain as an input to the μPB8214 in order to be serviced.

FUNCTIONAL DESCRIPTION

FUNCTIONAL
DESCRIPTION
(CONT.)

PRIORITY REQUEST	RST	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		1	1	$\overline{A_2}$	$\overline{A_1}$	$\overline{A_0}$	1	1	1
LOWEST	$\overline{R_0}$	7	1	1	1	1	1	1	1
	$\overline{R_1}$	6	1	1	1	1	0	1	1
	$\overline{R_2}$	5	1	1	1	0	1	1	1
	$\overline{R_3}$	4	1	1	1	0	0	1	1
	$\overline{R_4}$	3	1	1	0	1	1	1	1
	$\overline{R_5}$	2	1	1	0	1	0	1	1
	$\overline{R_6}$	1	1	1	0	0	1	1	1
HIGHEST	$\overline{R_7}$	0	1	1	0	0	0	1	1

CAUTION RST 0 will vector the program counter to location 0 (zero) and invoke the same routine as the "RESET" input to 8080A.

Current Status Register

The current status register is designed to prevent an incoming interrupt request from overriding the servicing of an interrupt with higher priority. Via software, the priority level of the interrupt being serviced by the microprocessor is written into the current status register on $\overline{B_0}$ - $\overline{B_2}$. The bit pattern written should be the complement of the interrupt level.

The interrupt level currently being serviced is written into the current status register by driving \overline{ECS} (Enable Current Status) low. The μ PB8214 will only accept interrupts with a higher priority than the value contained by the current status register. Note that the programmer is free to use the current status register for other than as above. Other levels may be written into it. The comparison may be completely disabled by driving \overline{SGS} (Status Group Select) low when \overline{ECS} is driven low. This will cause the μ PB8214 to accept incoming interrupts only on the basis of their priority to each other.

Priority Comparator

The priority comparator circuitry compares the level of the interrupt accepted by the priority encoder and request latch with the contents of the current status register. If the incoming request has a priority level higher than that of the current status register, the \overline{INT} output is enabled. Note that this comparison can be disabled by loading the current status register with $\overline{SGS}=0$.

Expansion Control Signals

A microcomputer design may often require more than eight different interrupts. The μ PB8214 is designed so that interrupt system expansion is easily performed via the use of three signals: ETLG (Enable This Level Group); ENLG (Enable Next Level Group); and \overline{ELR} (Enable Level Read). A high input to ETLG indicates that the μ PB8214 may accept an interrupt. In a typical system, the \overline{ENLG} output from one μ PB8214 is connected to the ETLG input of another μ PB8214, etc. The ETLG of the μ PB8214 with the highest priority is tied high. This configuration sets up priority among the cascaded μ PB8214's. The ENLG output will be high for any device that does not have an interrupt pending, thereby allowing a device with lower priority to accept interrupts. The \overline{ELR} input is basically a chip enable and allows hardware or software to selectively disable/enable individual μ PB8214's. A low on the \overline{ELR} input enables the device.

μPB8214

Interrupt Control Circuitry

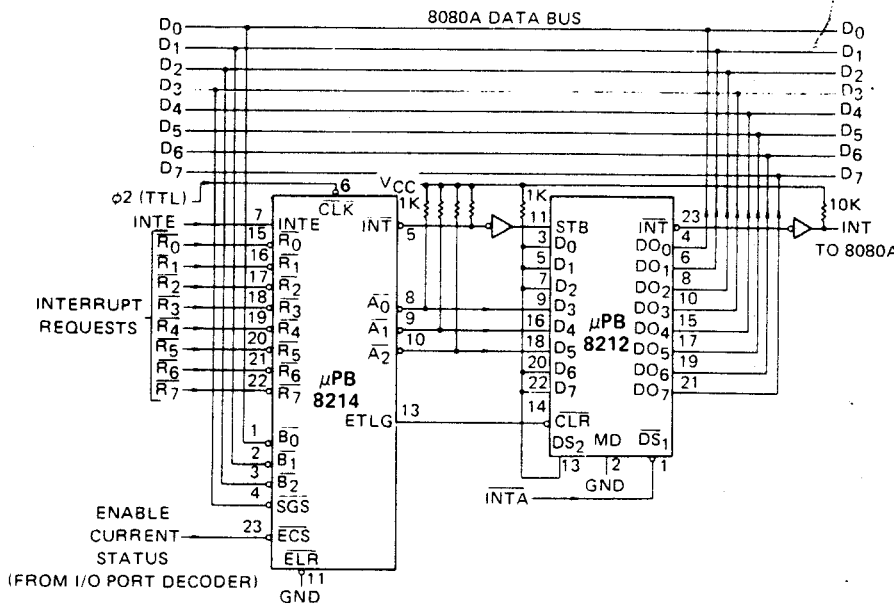
The μPB8214 contains two flip-flops and several gates which determine whether an accepted interrupt request to the μPB8214 will generate a system interrupt to the 8080A. A condition gate drives the D input of the interrupt flip-flop whenever an interrupt request has been completely accepted. This requires that: the ETLG (Enable This Level Group) and INTE (Interrupt Enable) inputs to the μPB8214 are high; the \overline{ELR} input is low; the incoming request must be of a higher priority than the contents of the current status register; and the μPB8214 must have been enabled to accept interrupt requests by the clearing of the interrupt disable flip-flop.

Once the condition gate drives the D input of the interrupt flip-flop high, a system interrupt (\overline{INT}) to the 8080A is generated on the next rising edge of the \overline{CLK} input to the μPB8214. This \overline{CLK} input is typically connected to the φ2 (TTL) output of an 8224 so that 8080A set-up time specifications are met. When \overline{INT} is generated, it sets the interrupt disable flip-flop so that no additional system interrupts will be generated until it is reset. It is reset by driving \overline{ECS} (Enable Current Status) low, thereby writing into the current status register.

It should be noted that the open collector \overline{INT} output from the μPB8214 is active for only one clock period and thus must be externally latched for inputting to the 8080A. Also, because the \overline{INT} output is open collector, when μPB8214's are cascaded, an \overline{INT} output from any one will set all of the interrupt disable flip-flops in the array. Each μPB8214's interrupt disable flip-flop must then be cleared individually in order to generate subsequent system interrupts.

FUNCTIONAL DESCRIPTION (CONT.)

TYPICAL μPB8214 CIRCUITRY



Parameter	Operating Range	Absolute Maximum Ratings*
Operating Temperature	0°C to +70°C	ABSOLUTE MAXIMUM RATINGS*
Storage Temperature	-65°C to +125°C	
All Output and Supply Voltages	-0.5 to +7 Volts	
All Input Voltages	-1.0 to +5.5 Volts	
Output Currents	100 mA	

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. ①	MAX.		
Input Clamp Voltage (all inputs)	V_C			-1.0	V	$I_C = 5\text{mA}$
Input Forward Current: ETLG input	I_F		-0.15	-0.5	mA	$V_F = 0.45\text{V}$
all other inputs			-0.08	-0.25	mA	
Input Reverse Current: ETLG input	I_R			80	μA	$V_R = 5.25\text{V}$
all other inputs				40	μA	
Input LOW Voltage: all inputs	V_{IL}			0.8	V	$V_{CC} = 5.0\text{V}$
Input HIGH Voltage: all inputs	V_{IH}	2.0			V	$V_{CC} = 5.0\text{V}$
Power Supply Current	I_{CC}		90	130	mA	②
Output LOW Voltage: all outputs	V_{OL}		.3	.45	V	$I_{OL} = 10\text{mA}$
Output HIGH Voltage: ENLG output	V_{OH}	2.4	3.0		V	$I_{OH} = 1\text{mA}$
Short Circuit Output Current: ENLG output	I_{OS}	-20	-35	-55	mA	$V_{OS} = 0\text{V}$, $V_{CC} = 5.0\text{V}$
Output Leakage Current: INT and A_0-A_2	I_{CEX}			100	μA	$V_{CEX} = 5.25\text{V}$

CAPACITANCE ④ $T_a = 25^\circ\text{C}$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. ①	MAX.		
Input Capacitance	C_{IN}		5	10	pF	$V_{BIAS} = 2.5\text{V}$
Output Capacitance	C_{OUT}		7	12	pF	$V_{CC} = 5\text{V}$ $f = 1\text{MHz}$

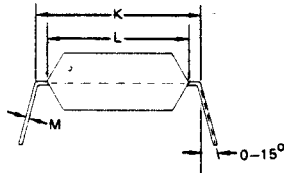
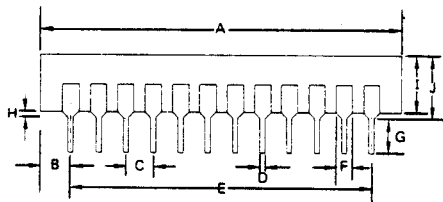
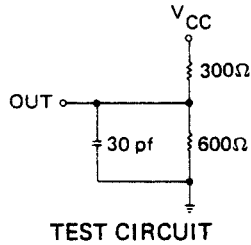
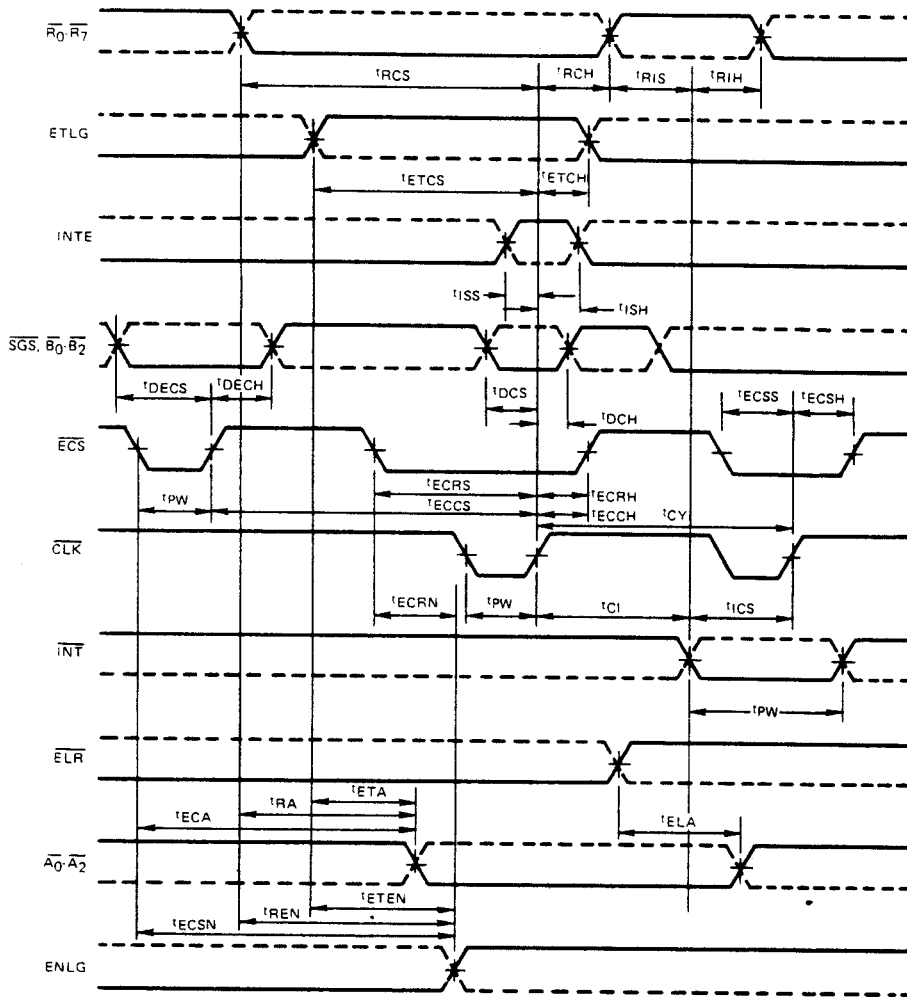
AC CHARACTERISTICS $T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. ①	MAX.		
CLK Cycle Time	t_{CY}	80	50		ns	Input pulse amplitude: 2.5 Volts
CLK, ECS, INT Pulse Width	t_{PW}	25	15		ns	
INTE Setup Time to CLK	t_{ISS}	16	12		ns	
INTE Hold Time after CLK	t_{ISH}	20	10		ns	Input rise and fall times: 5 ns between 1 and 2 Volts
ETLG Setup Time to CLK	t_{ETCS} ④	25	12		ns	
ETLG Hold Time After CLK	t_{ETCH} ④	20	10		ns	
ECS Setup Time to CLK	t_{ECCS} ④	80	50		ns	
ECS Hold Time After CLK	t_{ECCH} ⑤	0			ns	
ECS Setup Time to CLK	t_{ECSR} ⑤	110	70		ns	
ECS Hold Time After CLK	t_{ECRH} ⑤	0			ns	Output loading of 15 mA and 30 pF
ECS Setup Time to CLK	t_{ECSS} ④	75	70		ns	
ECS Hold Time After CLK	t_{ECSH} ④	0			ns	Speed measurements taken at the 1.5 Volts levels.
SGS and B_0-B_2 Setup Time to CLK	t_{DCS} ④	70	50		ns	
SGS and B_0-B_2 Hold Time After CLK	t_{DCH} ④	0			ns	
R_0-R_7 Setup Time to CLK	t_{RCS} ⑤	90	55		ns	
R_0-R_7 Hold Time After CLK	t_{RCH} ⑤	0			ns	
INT Setup Time to CLK	t_{ICS}	55	35		ns	
CLK to INT Propagation Delay	t_{CI}		15	25	ns	
R_0-R_7 Setup Time to INT	t_{RIS} ⑥	10	0		ns	
R_0-R_7 Hold Time After INT	t_{RIH} ⑥	35	20		ns	
R_0-R_7 to A_0-A_2 Propagation Delay	t_{RA}		80	100	ns	
ELR to A_0-A_2 Propagation Delay	t_{ELA}		40	55	ns	
ECS to A_0-A_2 Propagation Delay	t_{ECA}		100	120	ns	
ETLG to A_0-A_2 Propagation Delay	t_{ETA}		35	70	ns	
SGS and B_0-B_2 Setup Time to ECS	t_{DECS} ⑥	15	10		ns	
SGS and B_0-B_2 Hold Time After ECS	t_{DECH} ⑥	15	10		ns	
R_0-R_7 to ENLG Propagation Delay	t_{REN}		45	70	ns	
ETLG to ENLG Propagation Delay	t_{ETEN}		20	25	ns	
ECS to ENLG Propagation Delay	t_{ECRN}		85	90	ns	
ECS to ENLG Propagation Delay	t_{ECSN}		35	55	ns	

- Notes:
- ① Typical values are for $T_a = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$
 - ② B_0-B_2 , SGS, CLK, R_0-R_4 grounded, all other inputs and all outputs open.
 - ③ This parameter is periodically sampled and not 100% tested.
 - ④ Required for proper operation if INTE is enabled during next clock pulse.
 - ⑤ These times are not required for proper operation but for desired change in interrupt flip-flop.
 - ⑥ Required for new request or status to be properly loaded.

μPB8214

TIMING WAVEFORMS



**PACKAGE OUTLINE
μPB8214C**

ITEM	MILLIMETERS	INCHES
A	33 MAX.	1.28
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	3.2 MIN.	0.125 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	16.24	0.6
L	13.2	0.52
M	0.25 ± 0.1	0.01 ± 0.004